HIGH-SPEED DIFFERENTIAL FLIP-FLOP

Michael A. Nix

BACKGROUND

[0001] Logic circuits can be classified into two broad categories, combinational logic circuits and sequential logic circuits. The basic building block of sequential logic circuits is the flip-flop, also called a bi-stable multi-vibrator or latch. In most cases, logic circuits employ both sequential and combinational logic.

[0002] Figure 1 (prior art) depicts an exemplary logic circuit 100 that includes both combinational and sequential logic elements. Logic circuit 100 is a divide-by-five counter 100 with a pair of NOR gates 105 in a feedback path of a series of differential-input flip-flops 110. Circuit 100 receives a pair of complementary clock signals C and Cb, which extend to clock input terminals of each of the flip-flops 110. Circuit 100 produces a pair of complementary clock signals C/5 and Cb/5 with a frequency one fifth that of the input clock signals. The differential nature of circuit 100 allows for higher clock frequencies than would a similar divide-by-five circuit using single-ended sequential logic elements.

[0003] Figure 2 (prior art) depicts an embodiment of a differential-input flip-flop 110 for use in circuit 100 of Figure 1. The operation of flip-flop 110 is commonly understood by those of skill in the art, so a detailed description of flip-flop 110 is omitted here for brevity.

[0004] If manufactured using commonly available CMOS processes, flip-flop 110 can perform with clock frequencies as high as about 2 GHz. Unfortunately, modern high-speed digital communication systems employ clock and data recovery circuits operating in the 10Gb/s range. The

frequency response of flip-flop 110 is therefore insufficient to meet the needs of some modern systems.

SUMMARY

[0005] The present invention is directed to high-speed flip-flops. A flip-flop in accordance with one embodiment of the invention has a differential input stage that incorporates some combinational logic. This embodiment improves speed performance by reducing or eliminating the need for separate combinational logic circuits when the flip-flop is employed in certain circuit configurations. In one example, a flip-flop incorporating combinational logic is used in conjunction with other flip-flops to create a counter circuit that would otherwise require separate combinational logic.

[0006] A flip-flop in accordance with another embodiment of the invention includes differential input and output stages, each of which includes a transistor connected across its differential output terminals. The transistors are clocked to short the differential output terminals between expressions of logic levels, thereby limiting the maximum amount of voltage swing required to express subsequent logic levels.

[0007] This summary does not define the scope of the invention, which is instead defined by the appended claims.

A Brief Description of the Figures

[0008] Figure 1 (prior art) depicts an exemplary logic circuit 100 that includes both combinational and sequential logic elements.

[0009] Figure 2 (prior art) depicts an embodiment of a differential-input flip-flop 110 for use in circuit 100 of

Figure 1.

[0010] Figure 3 depicts a divide-by-five circuit 300 that divides a pair of complimentary clock signals C and Cb by five.

[0011] Figure 4 depicts a flip-flop 400 that is an embodiment of flip-flop 310 of Figure 3.

[0012] Figure 5 is a waveform diagram 500 depicting exemplary signals associated with the operation of flip-flop 400 of Figure 4.

[0013] Figure 6 depicts a flip-flop 600 that may be used in place of flip-flop 305 (Figure 3) in one embodiment of the invention.

[0014] Figure 7 depicts a differential circuit that can be used as circuit 315 of Figure 3 to convert the differential signal on terminals Q and Qb of the last flip-flop 310 in circuit 300 into full-swing, stable differential output signals.

DETAILED DESCRIPTION

[0015] Figure 3 depicts a divide-by-five circuit 300 that divides a pair of complimentary clock signals C and Cb by five. Like circuit 100 of Figure 1, circuit 300 employs differential signaling to improve performance. Circuit 300 differs from circuit 100, however, in that the logic associated with NOR gates 105 of Figure 1 is incorporated into a single flip-flop 305 adapted to receive two pairs of complimentary inputs D0, D0b and D1, D1b. The operation of an embodiment of flip-flop 305 is detailed below in connection with Figure 6.

[0016] Circuit 300 also includes a number of flip-flops 310 that are modified in accordance with the invention to improve speed performance. Finally, circuit 300 includes a

differential to single-ended converter 315. Flip-flops 310 and converter 315 are described below in connection with Figures 4, 5, and 7.

[0017] Figure 4 depicts a flip-flop 400 that is an embodiment of flip-flop 310 of Figure 3. Flip-flop 400 includes an input stage (left) and an output stage (right). The input stage includes a pair of differential transistors 400 and 405, the control inputs of which are connected to respective complementary data inputs D and Db. The output terminals X1 and X2 of the input stage connect to respective control terminals of a pair of differential transistors 410 and 415 in the output stage. The input and output stages include respective cross-coupled PMOS transistor loads 420 and 425.

[0018] The input stage includes an NMOS transistor 430 having one current handling terminal connected to output terminal X1 and the other connected to output terminal X2. The control input (gate) of transistor 430 is connected to the clock signal Cb. The output stage likewise includes a transistor 435, one current-handling terminal of which is connected to output terminal Q, the other current-handling terminal to output terminal Qb. The control terminal of transistor 435 is connected to clock signal C. In another embodiment, one of transistors 430 and 435 is substituted with a PMOS transistor, allowing both control terminals associated with transistors 430 and 435 to be controlled by the same clock signal.

[0019] Figure 5 is a waveform diagram 500 depicting exemplary signals associated with the operation of flip-flop 400 of Figure 4. Diagram 500 depicts complimentary clock signals C and Cb, data signals D and Db, input-stage output signals X1 and X2, and output terminals Q and Qb.

The various node labels refer to both the signal and the corresponding circuit node. Whether a given designation refers to a node or a signal will be clear from the context.

[0020] Prior to time T0, clock signal Cb is high, so transistor 430 connects output terminals X1 and X2 of the input stage of flip-flop 400. The logic 0 input on the differential terminals D and Db consequently produces only a relatively small voltage difference across terminals X1 and X2. Though limited by the on resistance of transistor 430, the voltage across terminals X1 and X2 does reflect a logic 0 (i.e., X1 > X2).

[0021] At time T0, clock signal Cb goes low, turning off transistor 430 to disconnect terminals X1 and X2. The voltage between terminals X1 and X2 thus increases, better representing the difference between input signals on terminals D and Db. Also at time T0, clock signal C goes high, causing transistor 435 to connect output terminals Q and Qb. The voltage difference between signals Q and Qb therefore diminishes. Though limited by the on resistance of transistor 435, the voltage across terminals Q and Qb continues to reflect a logic 0 (i.e., Q < Qb).

[0022] Next, at time T1, clock signal C returns low and complimentary clock signal Cb returns high. Respective transistors 430 and 435 consequently change states, so that terminals X1 and X2 are once again connected and terminals Q and Qb are disconnected. In this new state, terminals X1 and X2 begin to approach one another and output terminals Q and Qb swing away from one another to reflect the differential input signals to transistors 410 and 415.

[0023] Before the receipt of a new data bit on differential input terminals D and Db, the pairs of output

terminals X1,X2 and Q,Qb approach one another to limit the maximum amount of voltage swing required to move the differential output signal to the next logic bit. For example, the logic level expressed on output terminals Q and Qb from time T2 to time T4 switches from a logic 0 to a logic 1, and therefore requires a maximum voltage swing for each of output terminals Q and Qb. The present invention expedites the time required to make this transition by beginning to bring Qb low and Q high prior to receipt of the data signal indicating the logic transition. The resulting reduction in the maximum voltage swing required to change the logic level expressed on terminals Q and Qb reduces the maximum amount of time required to make logic transitions on terminals Q and Qb. This embodiment of the invention thus speeds the logic transitions on the outputs of flip-flop 310.

[0024] As illustrated between times T4 and T6, the voltage difference between terminals Q and Qb is reduced even if the next data bit turns out to be the same logic level as the one presently represented. This is because flip-flop 400 cannot anticipate the next logic level, and consequently must prepare for either of the two alternatives. Flip-flop 400 therefore requires some amount of time to "transition" between two logic zeroes or two logic ones. The overall speed of flip-flop 400 increases because the time required to transition between different logic levels is reduced.

[0025] Reducing the time required for flip-flop 400 to transition between different logic levels translates directly into improved speed performance. Moreover, as compared with flip-flop 110 (Figure 2), flip-flop 400 has far fewer transistors, and can therefore be implemented

using less die area. These changes also result in significantly reduced power consumption for a given level of speed performance.

[0026] Figure 6 depicts a flip-flop 600 that may be used in place of flip-flop 305 (Figure 3) in one embodiment of the invention. Flip-flop 600 is largely similar to flip-flop 310 of Figure 4, like numbered features being identical. Due to the similarities of flip-flop 600 and flip-flop 310, a detailed description of flip-flop 600 is omitted for brevity.

[0027] Flip-flop 600 is modified in accordance with an embodiment of the invention to receive two pairs of differential inputs D0,D0b and D1,D1b. As noted above in connection with Figure 1, NOR gates 105 impose some delay that slows the maximum operating speed of circuit 100 of Figure 1. Flip-flop 600 incorporates a pair of logic gates 605 and 610 that eliminate the need for NOR gates 105, and therefore speed up divide-by-five circuit 300 of Figure 3. Gate 605, composed of a pair of transistors 615 and 620, performs a NOR function of inputs D0 and D1; a pair of serial-connected transistors 625 and 630 within gate 610 performs a NAND function of input signals D0b and D1b.

[0028] As shown in Figure 5, the data output on complimentary output terminals Q and Qb fluctuates even when the data signal does not. Figure 7 depicts a differential circuit that can be used as circuit 315 of Figure 3 to convert the differential signal on terminals Q and Qb of the last flip-flop 310 in circuit 300 into full-swing, stable differential output signals.

[0029] While the present invention has been described in connection with specific embodiments, variations of these embodiments will be obvious to those of ordinary skill in

the art. For example, the invention can be adapted for use with other types of sequential logic elements, such as single-stage latches, toggle flip-flops, a J-K flip-flops, AND-input flip-flops, or XOR-input flip-flops. Moreover, some components are shown directly connected to one another while others are shown connected via intermediate components. In each instance, the method of interconnection establishes some desired electrical communication between two or more circuit nodes, or terminals. Such communication may often be accomplished using a number of circuit configurations, as will be understood by those of skill in the art. Therefore, the spirit and scope of the appended claims should not be limited to the foregoing description.